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| EXAMINER | |
|---|---|
| SONG, JASMINE | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2188 | |

DATE MAILED: 10/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 09/830,094 | BLIXT, SVEN STEFAN. |
| | Examiner | Art Unit |
| | Jasmine Song | 2188 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *amendment filed on 07/23/2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9 and 15-41* is/are rejected.

7)☒ Claim(s) *7,8 and 10-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## Detailed Action

1. This office action is in response to Amendment filed on 07/23/2004. Claims 1-41 are still pending in the application. All rejections and objections not explicitly repeated below are withdrawn.

## Specification

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

## Claim Objections

3. Claim 15 is objected to because of the following informalities:

Claim 15, lines 5, "a processor" should be changed to –the processor--.

Appropriate correction is required.

## Claim Rejections - 35 USC § 102

4. The rejections of claims 1-6,9 and 15-41 are maintained and newly added limitations are also rejected as shown below.

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-6,9, and 15-41 are rejected under 35 U.S.C. 102(e) as being anticipated by Satou et al., US. Patent 6,101,584.

Regarding claim 1, Satou et al. teaches that a method for controlling access to a dynamic random access memory (DRAM) in a computer system having a processor (Fig.1, CPU 110) and memory controller (memory controller 160), wherein said method comprises the step of performing a sequence of a predetermined number of DRAM control operations (it is taught as read or write access request to the DRAM region Fig.1, col.8, lines 2-4; col.23, lines 21 to col.24, lines 49) for each DRAM access, each DRAM control operation (read or write operation, such as operation code LOAD) being included in microcode instructions of the processor (each instruction include operation code and operands, for example, load instruction include operation code LOAD and operands. Please refer to Computer Architecture written by Mehdi R. Zargham, page 23-26).

Regarding claim 15, Satou et al. teaches that a controller (Fig.1, memory controller 160) for a dynamic random access memory (DRAM) (Fig.1, DRAM 120), in a compute system having a processor (Fig.1, CPU 110), wherein said DRAM controller is responsive to a sequence of control instructions for controlling access to said DRAM

(the memory controller is in responses to the read or write operation, such as operation code LOAD), each control instruction being included in a microcode instruction of the processor (each instruction include operation code and operands, for example, load instruction include operation code LOAD and operands. Please refer to Computer Architecture written by Mehdi R. Zargham, page 23-26).

Regarding claim 24, Satou et al. teaches that a computer system having a processor (Fig.1, CPU 110), a primary memory (Fig.1, DRAM 120) cooperating with said processor, and a memory controller (Fig.1, memory controller 160) for said primary memory, wherein said memory controller is responsive to a sequence of control instructions from said processor for controlling access to said primary memory (the memory controller is in responses to the read or write operation, such as operation code LOAD), each control instruction being included in a microcode instruction of said processor (each instruction include operation code and operands, for example, load instruction include operation code LOAD and operands. Please refer to Computer Architecture written by Mehdi R. Zargham, page 23-26).

Regarding claim 29, Satou et al. teaches that a method for performing a virtual direct memory access (DMA) to a primary memory in a computer system, wherein said method comprises the steps of:

storing data from/ to an input/output device (Fig.1 or Fig.2) in a buffer (it is taught as buffer 150h as shown in Fig.3, col.16, lines 50-57); transferring said data between

said buffer and said primary memory (it is taught as DRAM 120) via internal data paths of a processor of the computer system (it is taught as internal data bus 170 in Fig.1 and 2, col.14, lines 44-48), said data transfer being controlled by a microcode instruction program (each instruction include operation code and operands, for example, load instruction include operation code LOAD and operands. Please refer to Computer Architecture written by Mehdi R. Zargham, page 23-26) of the processor.

Regarding claim 36, Satou et al. teaches that a computer system having a processor (Fig.1, CPU 100) and a primary memory (Fig.1, DRAM 120) coupled to said processor, wherein said computer system further comprises: a buffer (it is taught as buffer 150h as shown in Fig.3, col.16, lines 50-57) for storing data from/to an input/output device (Fig.1, external bus controller); and means for transferring said data between said buffer and said primary memory via internal data paths of the processor (it is taught as internal data bus 170 in Fig.1 and 2, col.14, lines 44-48) under the control of a microcode instruction program (each instruction include operation code and operands, for example, load instruction include operation code LOAD and operands. Please refer to Computer Architecture written by Mehdi R. Zargham, page 23-26) in the processor.

Regarding claims 2 and 17, Satou et al. teaches that each microcode instruction includes a control instruction (it is taught as CTRLD, each Load operation need to have control instruction in order to access DARM), formed by at least one control bit (col.23,

lines 35-36), controlling which one of a plurality of predefined DRAM control operations to perform (col.23, lines 22 to col.24, lines 60).

Regarding claim 3, Satou et al. teaches that said predefined DRAM control operations are arrangeable to form said sequence of DRAM control operations such that a read access, a write access, a page mode read access, a page mode write access, a page mode read write access or a page mode write read access to said DRAM is enabled (col.23, lines 22 to col.24, lines 60).

Regarding claims 4 and 20, Satou et al. teaches that at least one control instruction in said sequence of control instructions temporarily puts the memory cycle of said DRAM on hold (col.24, lines 11-49, it is taught as hold request signal /HREQ).

Regarding claim 5, Satou et al. teaches further comprises the step of selecting the cycle time of each microcode instruction from a number of different cycle times such that the cycle time of each microcode instruction matches the duration of the corresponding DRAM control operation (Fig.6 to Fig.10; col.23, lines 22 to col.24, lines 49).

Regarding claim 6, Satou et al. teaches that each microcode instruction includes a cycle time control bit determining the cycle time of the microcode instruction, a first logical state of the cycle time control bit indicating a first cycle time and a second logical

state of the cycle time control bit indicating a second extended cycle time (col.21, lines 8-45).

Regarding claim 9, Satou et al. teaches that

characterized in that a third one, referred to as a H-operation, of said predefined DRAM control operations; includes the steps of:

deactivating a column address strobe (CAS) signal to said DRAM; and deactivating a write enable signal to said DRAM (col.24, lines 38-48).

Regarding claim 16, Satou et al. teaches that said DRAM controller (Fig.1, memory controller 160) controls access to said DRAM by performing a sequence of a predetermined number of DRAM control operations (Fig.1, col.8, lines 2-4; col.23, lines 21 to col.24, lines 49) in response to said sequence of control instructions (Fig.1, col.8, lines 56-58, it is taught as control signal CTRLD; col.23, lines 21 to col.24, lines 49).

Regarding claims 18 and 28, Satou et al. teaches that the cycle time of each microcode instruction is extendable such that the cycle time of each microcode instruction matches the duration of the corresponding DRAM control operation (Fig.6 to Fig.10; col.23, lines 22 to col.24, lines 49).

Regarding claim 19, Satou et al. teaches that the cycle time of each microcode instruction is extendable by means of a cycle time control instruction included within the microcode instruction itself (col.21, lines 8-45).

Regarding claim 21, Satou et al. teaches that the microcode instructions of said processor (it is taught as the microprocessor 100 in the Fig.1) are stored in a program memory (Fig.2, it is taught as instructions queue 110a) separated from said DRAM (Fig.1, DRAM 120).

Regarding claim 22, Satou et al. teaches that said DRAM controller (Fig.1, memory controller 160) is responsive to address information (an instruction fetch access address signal AF for specifying address of memory of the instruction fetch access), determined by a number of microcode instructions of said processor (col.7, lines 55-66), for addressing said DRAM (Fig.1, DRAM 120).

Regarding claim 23, Satou et al. teaches that the microcode instructions of said processor are the instructions of a reduced instruction set computing (RISC) processor (col.4, lines 34-38).

Regarding claim 25, Satou et al. teaches that said primary memory is a DRAM (col.4, lines 34-38), and said memory controller (Fig.1, memory controller 160) controls access to said DRAM by performing a sequence of DRAM control operations (Fig.1,

col.8, lines 2-4; col.23, lines 21 to col.24, lines 49) in response to said sequence of control instructions (Fig.1, col.8, lines 56-58, it is taught as control signal CTRLD; col.23, lines 21 to col.24, lines 49).

Regarding claim 26, Satou et al. teaches that said processor (Fig.1, CPU 110 within microprocessor 100) and said DRAM (DRAM 120) are provided on the same circuit board (Fig.1).

Regarding claim 27, Satou et al. teaches that said processor is a complex instruction set computing (CISC) processor (it is one of two major microprocessor design, the instructions can be very powerful, allowing for complicated and flexible ways of calculating such elements as memory addresses), and complex instructions are stored in said primary memory and executed by microcode instructions (it is taught as microprocessor generate the microcode instructions) stored in a program memory (Fig.2, instruction queue 110a) in said processor.

Regarding claims 30 and 37, Satou et al. teaches that said means for transferring data between said buffer and said primary memory includes: means for transferring data between said buffer (it is taught as the buffer 150h as shown in Fig.3) and an internal register (it is taught as 110d) of said processor in response to control signals generated by said microcode instruction program (Fig.1, col.8, lines 56-58, it is taught as control signal CTRLD; col.23, lines 21 to col.24, lines 49); and means for transferring

data between said internal register and said primary memory in response to a sequence of control instructions included in microcode instructions of said microcode instruction program (Fig.1, col.8, lines 56-58).

Regarding claims 31 and 39, Satou et al. teaches that said primary memory is a dynamic random access memory (DRAM) (it is taught as DRAM), and said means for transferring data between said internal register (it is taught as data buffer 110d) and said DRAM includes a DRAM controller (it is taught as memory controller 160) for performing a sequence of DRAM control operations (Fig.1, col.8, lines 2-4; col.23, lines 21 to col.24, lines 49) in response to said sequence of control instructions (Fig.1, col.8, lines 56-58, it is taught as control signal CTRLD; col.23, lines 21 to col.24, lines 49).

Regarding claim 32, Satou et al. teaches that said method further comprises the step of regularly investigating whether a predetermined amount of data is present in said buffer for inputs to the primary memory, and whether there is a predetermined amount of free space available in said buffer for outputs from the primary memory, said transfer between said buffer and said primary memory being initiated in dependence upon the outcome of said investigation (col.14, lines 28-43 and lines 47-47).

Regarding claim 33, Satou et al. teaches that said investigating step is performed by at least one microcode instruction that is activated at a predetermined frequency (col.14, lines 56 to col.15, lines 39).

Regarding claims 34 and 40, Satou et al. teaches that said microcode instruction program (Fig.2, it is taught as instructions queue 110a) of said processor (it is taught as the processor 110 in the Fig.1) is configured for performing at least one of processing (such as data decoding as shown in Fig.2) and monitoring of data transferred between said buffer (it is taught as the buffer 150h as shown in Fig.3) and said primary memory (it is taught as DRAM 120) via the internal data paths of said processor (it is taught as internal data bus 170 in Fig.1 and 2, col.14, lines 44-48).

Regarding claims 35 and 41, Satou et al. teaches that said processing comprises at least one of the following: data conversion, data encoding, data decoding, image data compression, image data decompression, scaling, pattern matching and checksum calculation (it is taught as data decoding as shown in Fig.2).

Regarding claim 38, Satou et al. teaches that said means for transferring data between said buffer (it is taught as the buffer 150h as shown in Fig.3) and said internal register (it is taught as 110d) includes a DMA controller (Fig.2, CPU control circuit 110j), which also controls transfer of data between said input/output device and said buffer (Fig.1 or Fig.2).

## Response to applicant's Arguments

7. Applicant's arguments filed 07/23/2004 have been fully considered but they are not persuasive.

In response to applicant's arguments "the CPU does not know in advance which type of memory access to be performed by the memory controller" on page 2 of Remarks, however, the Examiner noticed that this limitation is not in the claim, and therefore, this limitation is not being considered by the Examiner. Also, the applicant's argument " the memory accesses can never be controlled by the CPU, but rather is controlled by the memory controller", this is not true, the LOAD operation within CPU is directly controlled by the CPU, not controlled by memory controller (Please refer to Computer Architecture written by Mehdi R. Zargham, page 23-26).

In response to applicant's arguments "the control signals CTRLD or CTRLC used in Satou are not included in any instruction of the processor, but are generated by the memory controller and the computer system of Satou does not perform a sequence of DRAM control operations in response to a corresponding sequence of control instructions included in microcode instruction of the processor" and "the instructions stored in the instruction queue 110a of Satou are not microcode instructions" and "the register 110d is not used by peripheral input/output devices to store data" on page 3 and 5 of Remarks, however, the Examiner noticed that these limitations are taught by Satou, please refer back to the rejection above (since the applicant broadly claimed, these limitations can be interpreted in different way).

## Allowable Subject Matter

8. Claims 7-8 and 10-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

## Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. When responding to the office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 C.F.R. 1.111 (c).

11. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jasmine Song whose telephone number is 703-305-7701. The examiner can normally be reached on 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 703-306-2903. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Jasmine Song

Patent Examiner

October 14, 2004

Mano Padmanabhan

Supervisory Patent Examiner

Technology Center 2100

10/17/04

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER